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Thermal Test of an Improved Platform for Silicon Nanowire-Based Thermoelectric Micro-generators

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This work reports on an improved design intended to enhance the thermal isolation between the hot and cold parts of a silicon-based thermoelectric microgenerator. Micromachining techniques and silicon on insulator substrates are used to obtain a suspended silicon platform surrounded by a bulk silicon rim, in which arrays of bottom-up silicon nanowires are integrated later on to join both parts with a thermoelectric active material. In previous designs the platform was linked to the rim by means of bulk silicon bridges, used as mechanical support and holder for the electrical connections. Such supports severely reduce platform thermal isolation and penalise the functional area due to the need of longer supports. A new technological route is planned to obtain low thermal conductance supports, making use of a particular geometrical design and a wet bulk micromachining process to selectively remove silicon shaping a thin dielectric membrane. Thermal conductance measurements have been performed to analyse the influence of the different design parameters of the suspended platform (support type, bridge/membrane length, separation between platform and silicon rim,) on overall thermal isolation. A thermal conductance reduction from 1.82 mW/K to 1.03 mW/K, has been obtained on tested devices by changing the support type, even though its length has been halved.

Key words: Microgenerator, thermoelectricity, harvesting

INTRODUCTION

Most of world's power use is generated by means of heat engines using fossil fuel combustion, but almost two-thirds of the energy that is fed into these systems radiates away, becoming a waste heat source.[1] Thermoelectric modules, which have the capability of converting heat into electricity, have been proposed as a promising solution to turn this waste heat into useful power. Although recent research has been intensely exploring new materials and technical routes to boost the efficiency of such devices, thermoelectric energy conversion still represents a major scientific challenge towards an effective waste heat recovery. Several high-performance thermoelectric materials, such as Bi-Te based alloys, skutterudite compounds, Ag-Pb-Sb-Te quaternary systems and half-Heusler compounds[2–6] have been lately reported as efficient thermoelectric materials, but they are known to be scarce and expensive, toxic in some cases, as well as difficult to integrate in microelectronics. Alternative developments focus on the smart structuring of mainstream microelectronic materials as a route to achieve silicon-based thermoelectric generators. Individual silicon nanowires (Si NWs) have shown an enhanced thermoelectric performance over that of the bulk silicon ($ZT \sim 0.01$).[7,8] However, even though improved ZT values have been reported, the discussion around whether this nanomaterial will enable the production of competitive thermoelectric devices is still open. Our aim is to work towards an all-Si thermal generator by designing thermally

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efficient silicon microplatforms suitable for the subsequent monolithic integration of bottom-up Si NWs as thermoelectric active material.

DESIGN AND FABRICATION

The planar configuration proposed for the silicon-based thermoelectric microgenerator uses a silicon on insulator (SOI) substrate and silicon micromachining techniques to define a thermally isolated suspended Si platform surrounded by a bulk Si rim. Both parts are subsequently linked by means of Si NW arrays that are grown on a CVD reactor using a bottom-up vapour–liquid–solid (VLS) process.[9] In our previous work, the suspended platform was linked to the bulk Si rim by means of bulk Si bridges, in addition to the Si NW arrays, acting as mechanical support and as a holder for the electrical connections.[9–11] However, this kind of support severely reduces the platform thermal isolation due to the high thermal conductivity of the bulk Si, limiting the device ability to get a large temperature gradient from a waste heat source. Hence, long bridge supports are needed to develop large thermal gradients and significant device area is wasted giving rise to poor power densities. In this work, a new technological route has been set-up to increase the platform thermal isolation by replacing such silicon bridges by thin dielectric membranes, with a much lower thermal conductivity, which are used to support the metallic electrical connections. A particular geometrical design is proposed to etch the Si under the membrane area using a short wet bulk micromachining process, which is enough to shape these suspended low thermal conductance thin membranes and, at the same time, improve the surface quality of the ⟨111⟩ vertical walls where the Si NWs will be grown. A sketch of both designs is shown in Fig. 1.

They consist of a suspended silicon platform (S1) that will be later connected to a bulk silicon rim (S2) with Si NWs arrays. In former designs, the electrical connections were placed on top of bulk silicon bridges while in the new design proposed as an alternative they are laying on a thin dielectric membrane. The Si NWs will be grown perpendicular to the ⟨111⟩ walls that have been used to define the different Si parts on the SOI device layer. The temperature difference attainable across such devices when operated in harvesting mode (placed on top of a heat source) will essentially depend on the length of the thermoelectric material connecting the high- and low-temperature areas, which is technologically limited by the tapering effect during NWs growth.[12–15] Trenches for the successive linkage of multiple Si NW arrays have been developed in order to overcome this problem, providing larger effective Si NW lengths. A detailed schematic of the intended final structure is shown in Fig. 2. The fabrication is performed on SOI wafers, with thicknesses of the Si device layer, buried oxide layer and handle Si wafer of 15 μm, 0.5 μm, and 500 μm, respectively. Due to the peculiarity of Si NWs growth, which takes place predominantly along the ⟨111⟩ direction, a (110) surface orientation is selected for the SOI device layer surface, so that ⟨111⟩ planes can be exposed on vertically etched trenches. In contrast, the orientation of the SOI silicon handle wafer does not play any role and a standard (100) orientation is used.

The fabrication process starts with the deposition of a 300 nm thick LPCVD Si_3N_4 layer, to be used as mechanical support for the metals. After patterning this nitride layer using photolithography and a dry etch process, the metallization used to simultaneously obtain the electrical connections with the silicon device layer and a built-in heater element (electrically isolated from the silicon by the nitride film) was performed using a 30 nm thick titanium/tungsten (Ti/W) (10/90%) adhesion layer and a 200 nm thick W layer deposited by sputtering. A second photolithography and a wet etch were used to pattern the metal. Once the different metal structures are patterned the surface is protected with a 1 μm thick SiO_2 layer deposited by PECVD. The last step on the SOI device layer is to define the silicon structures, i.e. the isolated platform and the trenches that will enclose the Si NWs. This is done with a photolithographic step and a dry etch process that sequentially removes the SiO_2 and the silicon device layer, until the buried oxide layer is reached. Next, a short (150 s) KOH etch step was performed on the wafer top side to release the nitride bridge. This new step is critical, as it must remove the exposed Si

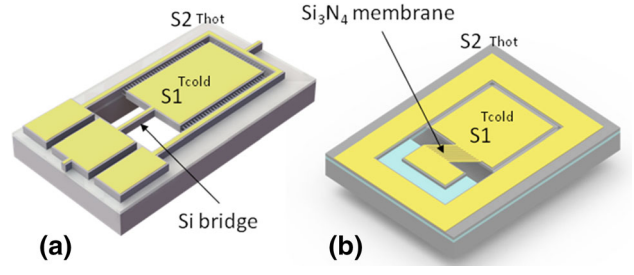

Fig. 1. Illustration of the microgenerator designs, classic (*a*) and proposed alternative (*b*). The isolated silicon mass (S1) is linked to bulk Si (S2) by means of a Si bridge (*a*) or alternatively by a thin dielectric membrane (*b*) with lower thermal conductance. For both designs, the area of the suspended platform is 1 mm × 1 mm. Bridge and membrane lengths are 200 μm and 100 μm, respectively.

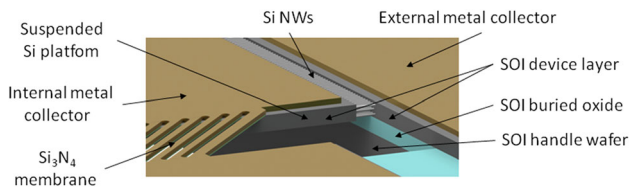

Fig. 2. Detailed device illustration showing the integration of the Si NWs on the SOI based structure. The featured area is a magnification of the [support membrane-platform-rim] region on Fig. 1 (right). The length of the Si NWs is 10 μm.

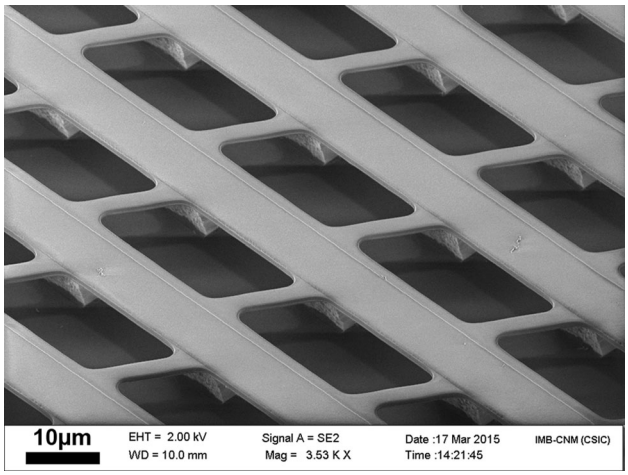

Fig. 3. SEM image of the supporting membrane after the KOH etch. Metal connections are sandwiched in a thin dielectric membrane, which is released by the silicon under-etch. Only small isolated Si islands remain.

device layer only under the nitride/metal/oxide bridge, while preserving the other device functional parts. In view of that, the membrane structure and the etch holes have been designed with a specific angle to allow a fast Si under-etch, while permanent Si parts are preserved as vertical walls have been aligned with ⟨111⟩ planes, which present a much slower etch rate when exposed to KOH. The SEM image of the bridge in Fig. 3 clearly shows that only small Si islands, which are isolated from each other, remain under the bridge after this short KOH step. This wet etch process plays and additional role, as it helps to restore the surface quality of the ⟨111⟩ vertical walls where Si NWs will be grown, removing the scalloping effect of the previous RIE etch (Bosch process). Devices are completed by processing the backside, using a 1 μm thick patterned aluminum layer that acts as a hard mask for a DRIE process that etches the handle wafer and the buried oxide layer. This process sequence is intended to build the different parts of the thermoelectric generator, maintaining all metals and silicon surfaces covered by SiO_2, except the Si vertical walls that expose the ⟨111⟩ planes for the silicon nanowire growth.

RESULTS AND DISCUSSION

A set of different devices has been produced using the described fabrication route. In addition, devices with the former bulk Si bridge supports have been produced (Fig. 4) to be used as reference to evaluate the improvement attained in the thermal isolation of the suspended platforms. Devices with two different bridge lengths (100 μm and 200 μm) and with different number of trenches (1–4) have been fabricated using the new membrane-like supports.

Figure 5 shows a detail of the multiple trenches used to increase the effective NW length. Each trench is 10 μm wide and midway silicon bars (3 μm wide) are used to define consecutive trenches. Configurations for test purposes have been created including a built-in heater (isolated from Si by the Si_3N_4 layer) to characterize the thermal isolation by forcing a controlled thermal gradient by Joule heating.

The thermal isolation achieved with the different designs has been assessed by measuring the total thermal conductance between the bulk silicon and the isolated platform, which accounts for the thermal conductivity of the different heat paths that connect both elements, i.e. the support (Si bridge or dielectric membrane), the Si bars that define the Si NW trenches and the surrounding air. Thermal conductance has been obtained using the integrated heater to dissipate a known power on the isolated platform and to simultaneously measure the developed temperature gradient. For this purpose, the temperature coefficient of the resistance (TCR) was previously measured for the heater material (1950 ± 25 ppm/°C) to calibrate the heater as a thermometer.

First of all, the performance of the new supports was compared with that of former bulk Si bridges. A classic design using two 200 μm long bridges has been compared with a new design using a shorter 100 μm long dielectric membrane, with a single trench (T1) for both devices. Figure 6 shows the temperature reached in the isolated platform as a function of the power dissipated in the heater element. Despite the reduced length, the membrane outperforms the bridge supports in terms of thermal isolation. Thermal conductance is almost halved, from 1.82 mW/K to 1.03 mW/K, pointing out that bridge conductance was the main contribution to total thermal conductance in old designs, turning into a limiting factor for thermoelectric performance.

Next, the influence of the distance between the isolated platform and the bulk silicon rim in the active area (the effective NW length) has been analyzed using a set of four devices featuring a 100 μm long dielectric membrane support and the four different trench designs (T1–T4). Figure 7 shows the temperature reached in the isolated platform as a function of the power dissipated in the heater element. As anticipated, the number of trenches has a significant effect on thermal isolation since thermal conductance is reduced from 1.03 mW/K for T1 to 0.68 mW/K for T4, the more numerous the trenches, the better the thermal isolation. The observed trend and values point out that the conductance of these bars is the main contribution to total thermal conductance in the new membrance designs. However, the thermal conductance of these trenches once filled with NWs in real thermoelectric generators will depend also on the parameters used for NW growth, which determine NW size and density. A complete optimization will be necessary to find a NW distribution and a num-

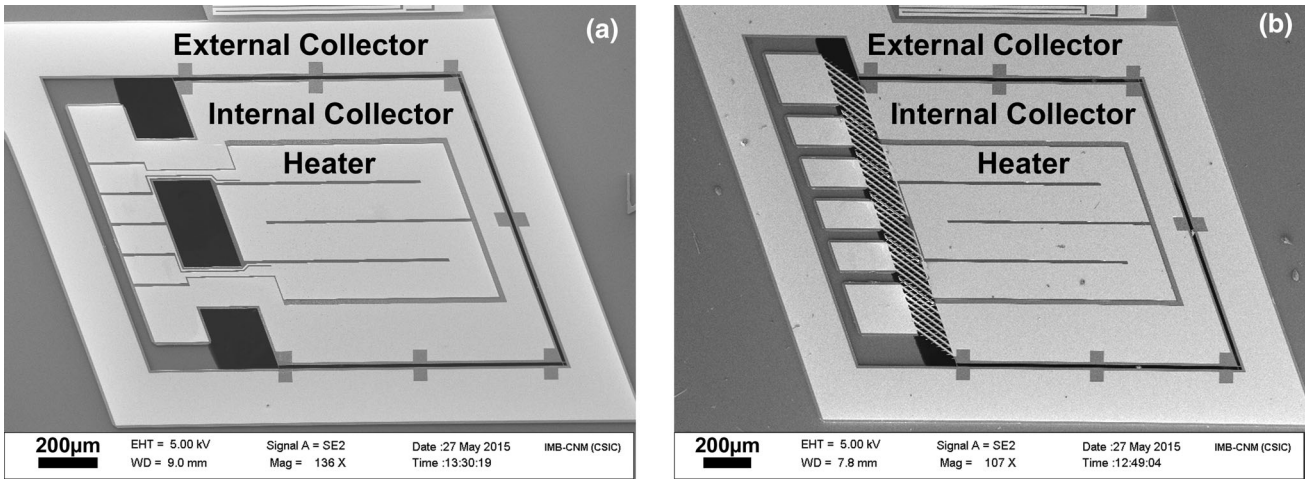

Fig. 4. SEM images showing the microfabricated platforms, with bulk Si (a) or thin dielectric (b) supports. Both are single trench devices and include a heater element for characterization purposes.

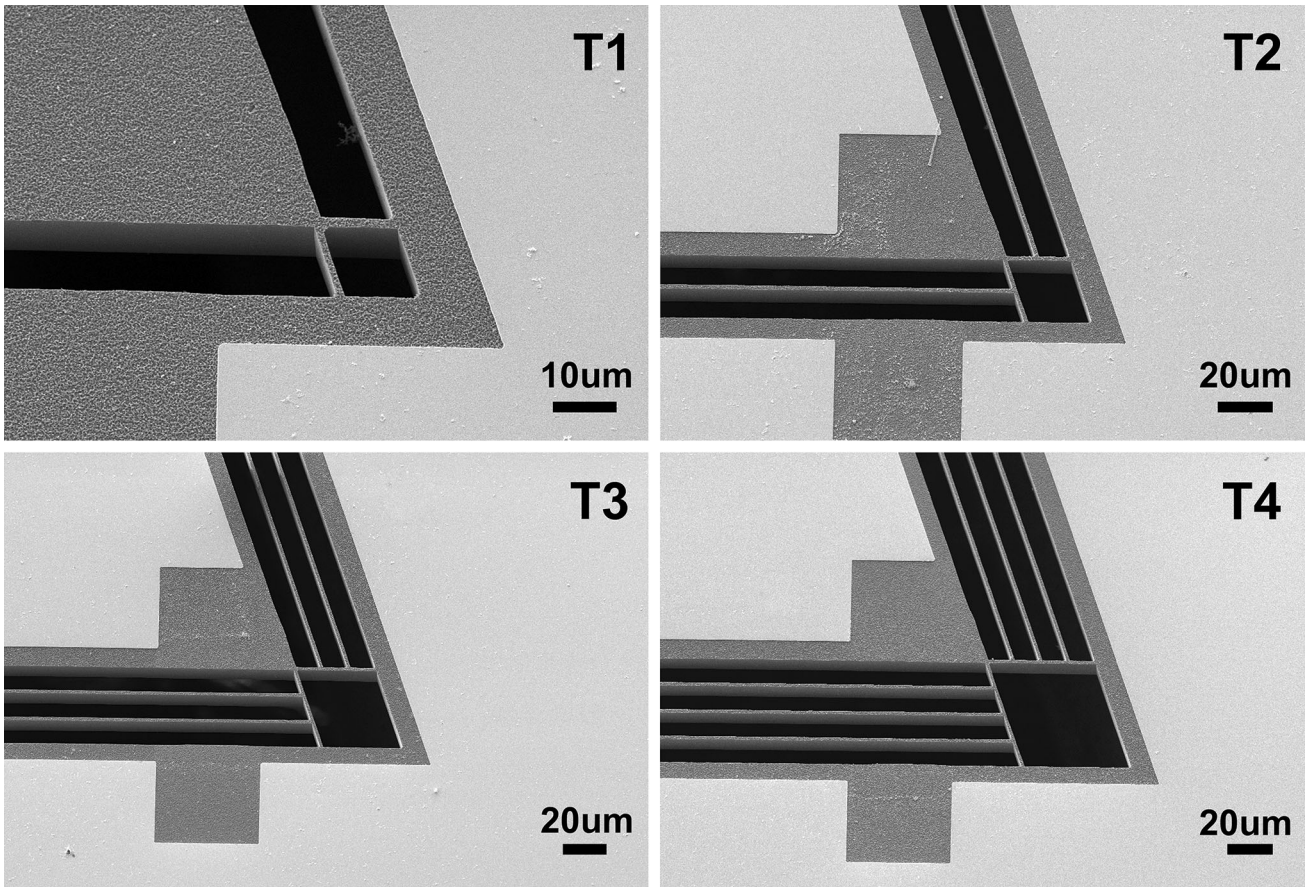

Fig. 5. SEM images of the silicon structures used to increase the effective nanowire length, from 10 μm (T1) to 40 μm (T4), with successive trenches to be filled with Si NWs. The images are a magnification of the bottom-right region of the platform-rim area featured in Fig. 4.

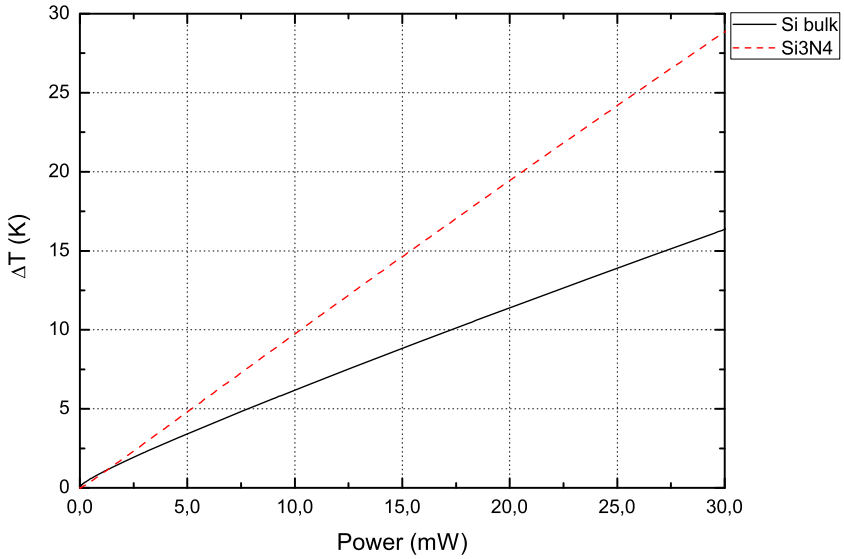

Fig. 6. Temperature increase in the platform as a function of dissipated power for two devices with a single trench, one with 200 μm long bulk Si supports (black) and other with a 100 μm long Si_3N_4 membrane (red) (Color figure online).

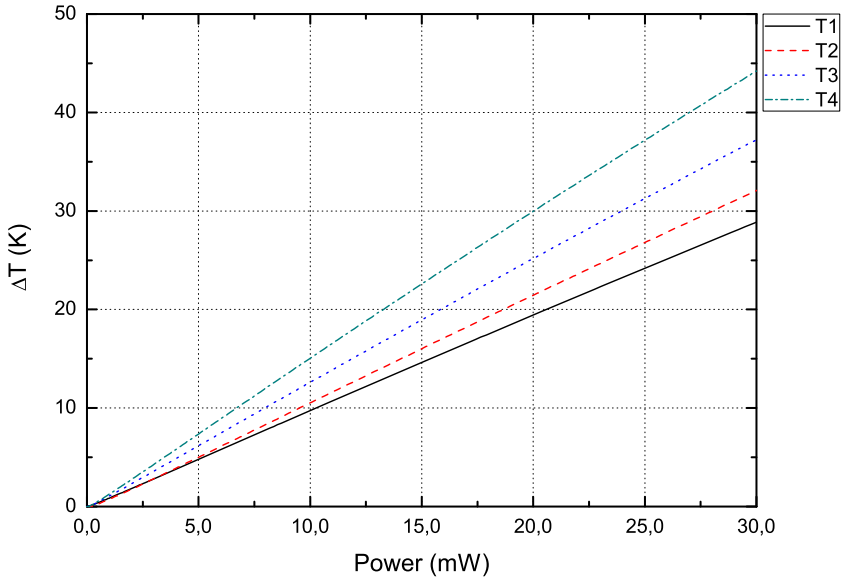

Fig. 7. Temperature increase in the platform as a function of dissipated power for devices with a 100 μm long Si_3N_4 membrane and different numbers of consecutive trenches (T1–T4) (black, red, blue, green) (Color figure online).

ber of trenches enhancing the thermoelectric performance, which shows an opposite dependency on thermal and electrical conductions.

Finally, the influence on thermal conductance of the length of the membrane support has been analyzed using a set of two devices with 100 μm and 200 μm long dielectric membranes (B1, B2), and the four trenches design (T4). Figure 8 shows the temperature reached in the isolated platform as a function of the power dissipated in the heater element. The small change observed in total thermal conductance, from 0.68 mW/K for B1 to 0.65 mW/K for B2, after having halved the contribution coming from the membrane support, confirms that main contribution to thermal conductance in new designs is linked to the silicon bars used to define the trenches to be filled with Si NWs, as anticipated in the previous measurement.

In the light of abovementioned improvement in thermal conductance, the new platform designs are expected to generate higher power densities than current devices using bulk Si bridges, which generated a maximum power density of 9 $\mu W/cm^2$ for $\Delta T = 27°C$.[9]

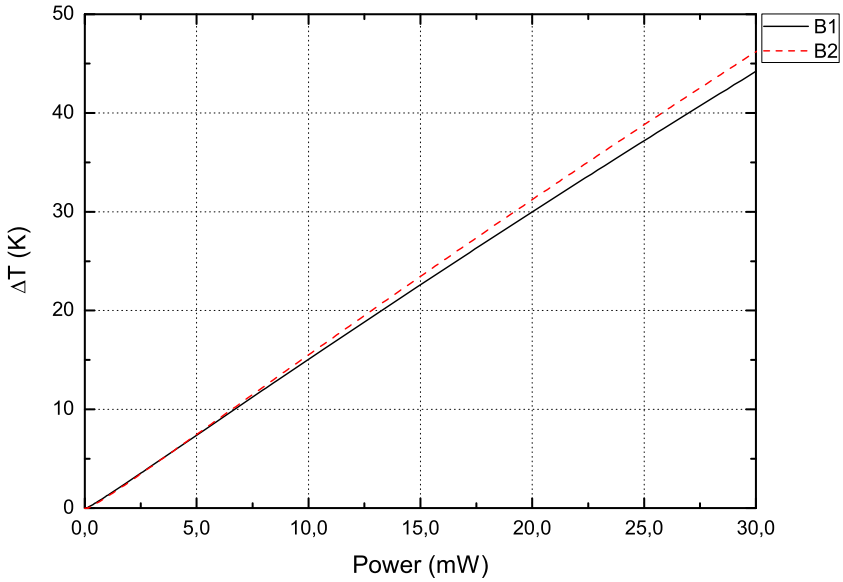

Fig. 8. Temperature increase in the platform as a function of dissipated power for two devices with 100 μm (B1, black) and 200 μm (B2, red) long Si_3N_4 membrane and four consecutive trenches (Color figure online).

CONCLUSIONS AND FUTURE WORK

A new technological route has been proposed to integrate low thermal conductance supports with the silicon micromachined suspended platforms used to build all-Si thermoelectric microgenerators. A set of devices based on this process have been successfully fabricated and thermal measurements have revealed that a significant thermal conductance reduction is attained with this membrane-like supports, even though shorter lengths are used. This result paves a route to further improve the power density attained with the all-Si microgenerators based on Si NWs. The compatibility of the supports with the Si NWs growth process has to be confirmed, and the thermal conductance of the supports has to be contrasted with that of the NWs arrays in order to establish the optimum length for this new type of support (i.e., the attainable support area reduction).

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